# **SUMMARY OF QUALIFICATIONS**

Highly versatile and self-motivated individual with 18+ years of experience focused on Verification and Design of complex digital designs. Experienced in managing people and leading teams. Ability to excel under pressure and enthusiastic to meet new challenges.

# **VERIFICATION SKILLS**

* Architected and implemented object oriented Constrained Random System Verilog UVM/OVM based verification environments for Complex Digital Design SoCs. Worked on Vera and Specman based verification environments.
* Very knowledgeable in System Verilog, Verilog, UVM (Universal Verification Methodology), OVM (Open Verification Methodology), constrained random stimulus generation, Functional Coverage definition and Closure, Scoreboarding, self-checking environments.
* Very good experience architecting DV environments, bus functional modeling, and DFT Verification including Production Test Vector generation.
* Quality & Schedule Driven Verification, Experienced with full verification Life Cycle.
* Very Good at Emulation, FPGA, ASIC Hardware Bring up, Validation
* Strong Debugging Skills.
* Technical Leadership and Global Team Building
* Very knowledgeable in Formal Verification using PSL assertions.
* Total 15+ years of Verification Experience

# **DESIGN SKILLS**

* Expertise in micro-architecture, RTL Design and Verilog RTL & Behavioral Coding.
* Very good experience at Low Power Designs and Multi-Clock Domain Designs.
* Excellent debugging skills.
* Good experience at Timing Analysis, ASIC synthesis, FPGA synthesis and Logic Equivalence Checking.
* Good experience in debugging designs both in ASIC and FPGA.
* Total 4+ years of Design Experience

# **DESIGN AND VERIFICATION TOOL SKILLS**

HDL & Verification Languages : System Verilog/Verilog, PSL Assertions, UVM,

OVM, VERA, Specman E, VHDL.

Programming Languages : C, C++, PERL, Python, TCL/TK

Protocols : AXI3/4, AHB, PCIe, Toggle NAND, DDR3/4,

PCI, USB, NVMe, Bluetooth, OCP, SAS, I2C,

UART

EDA Tools : VCS, NC-Sim, Questa, Verdi, Simvision,

DVE, 0-IN, Xilinx, Synplify Pro, Spyglass,

DC, PT-PX, Tetrmax, Veloce 2.

Build Management : Make, Clearcase, Perforce, CVS, Design Sync,

SVN

System Administration : Linux, Solaris, EDA CAD tool Admin

# **EMPLOYMENT HISTORY**

*Toshiba Memory America, San Jose, CA*

*Sr Staff Verification Engineer, Sept 2017-Till Date*

* UVM based Constraint random DV environment creation along with Testplan creation and execution for Data Center SSD Controller's Flash Interface SS block at Chip level and Sub System level. Helping FPGA/Palladium verification and validation.

*SK Hynix memory solutions, San Jose, CA*

*Sr Staff Verification Engineer, April 2013-Aug 2017*

* UVM based Constraint random DV environment creation along with Testplan creation and execution for Enterprise and Client SSD Controller's Flash Interface SS block at Chip level and Sub System level. Helping FPGA/Veloce verification and validation.

*SmartPlay Inc, San Diego, CA(Consultant at Qualcomm)*

*Principal Verification Engineer, December 2012-April 2013*

* UVM based Constraint random DV environment creation along with Test plan creation and execution for Peripheral SS block at Chip level and Sub System level. Guiding cross-site development teams in US and India.

*STEC Inc., San Diego, CA*

*Senior Staff Verification Engineer, December 2010- November 2012*

* Developed innovative methodologies that demonstrated quantifiable improvement in Quality and Time. Verification lead responsible for both Chip and Sub System Levels.
* UVM/OVM based Constraint random DV environment creation along with Test plan creation and execution for Multiprocessor based Flash SSD Controller Chip level and Sub Systems. Guiding cross-site development teams in US, Malaysia and Taiwan.

*RapidBridge LLC Inc. (QuantumThink Group, Inc.), San Diego, CA*

*Principal Engineer, July 2008- November 2010*

* NAV Core DV environment creation in OVM, Test plan creation and execution.
* OVM based Constraint random DV environment creation along with updating the existing C/Verilog DV environment for Power PC based SSD SOC, guiding cross-site development teams in US, Malaysia and Taiwan.
* Digital Design, DFT Scan design for the RF and Analog signal Chipsets.
* Complete DV environment development, Test plan, Implementation plan creation and Verification of Sub Systems using Verilog and also AMS simulations.

*QuantumThink(Qthink) Technologies Pvt Ltd., Bangalore,*

*Senior IC Design Engineer, May 2006-July 2008*

* Complete DV environment development, Test plan, Implementation plan creation and Verification of 6 Sub Systems using System Verilog and VMM.

*Sasken Communication Technologies, Bangalore,*

*Project Leader, June 2005-April 2006*

* Porting of ASIC RTL to FPGA, FPGA rtl Synthesis using Synplyfy Pro, P&R and Bit file generation for XILINX FPGA and verifying functionality using the generated bit files on board level.
* Worked closely with new team, executed the project at onsite and also at customer place, delivered to customer on time.
* Achieved the internal best team award.

*Alliance Semiconductor, Hyderabad,*

*Engineering Manager, March 2005-June 2005*

* Implemented Verilog/C/Perl based verification environment to verify PCI Express Bridge Chip. Test plan creation.

*Moschip Semiconductor Technologies, Hyderabad,*

*Senior Staff Engineer Verification, April 2002-March 2005*

* Build and Managed Strong Verification team.
* Successfully taped out 16 ASICs without functional bugs. 1 ASIC had minor bug.
* Lead teams from project requirements phase to the release and maintenance phase.
* Functional Production test vectors generation of all ASICs.

*Exanet Technologies, Bangalore,*

*Senior Design Engineer, Feb 1999 – March 2002*

* Micro-Architecture and Design of Bluetooth BaseBand IP core with AMBA ASB interface and PCI Interface, Integrated with TriMedia ChipSet.
* 2nd Generation Trimedia VLIW processor based set top box Full Chip Verification.
* DFT verification for Network Processor.

# **RELEVANT PROJECTS**

***Data Center SSD Controller SoC Verification:*** UVM based Configurable DV environment and Testbench creation for Data Center SSD Controller SoC which has PCIe Host, DDR3/4-LPDDR3/4 interface, Toggle NAND Flash interface, and peripheral ports like SDIO, UART, and SPI interfaces. My responsibility is to create top and block level dv environment creation along with the verification of Toggle NAND interface, FCT Block subsystem Command Controller.

***ARM Based Enterprise/Client/Mobile SSD Controller SoC Verification:*** UVM based Configurable DV environment and Testbench creation for Enterprise/Client/Mobile SSD Controller SoC which has PCIe/SATA Host, DDR3/4-LPDDR3/4 interface, Toggle NAND Flash interface, eMMC5.0, and peripheral ports like SDIO, UART, and SPI interfaces. My responsibility is to create top and block level dv environment creation along with the verification of Toggle NAND interface, FCT Block subsystem Command Controller which has configurable LinkedList IOP elements and configurable LinkedList Queues.

***Peripheral SS Verification:*** UVM based DV environment creation for Configurable Peripheral Subsystem which has USB3.0 Host, Device, USB2.0 Host, Device, eMMC5.0 Controller, SDIO Controller, UART, SPI and Parallel Port Controller interfaces. My responsibility is to create top level dv environment creation along with the verification of eMMC5 interface.

***PowerPC and ARC processors based SSD SOC:*** UVM based DV environment creation for 1 ARM and 6 ARC processors based SSD Controller. My responsibility is to create top level dv environment creation along with the verification of LDPC CodeWord Machine block using OVM and Flash interface verification.

***NAV Core Verification:*** OVM based Block level DV environment creation, test plan creation and execution for Clocks, BP1, BP2, BP2 and BP4 blocks. Also ported block level tests to Chip level DV, which is also in OVM.

***Power PC based SSD SOC:*** Challenging and highly complex DV project with limited resources and time. Guiding DV team, which is new to OVM and system Verilog. Work with team to enhance the current C/Verilog testbench along with OVM based DV environment architecture and implementation for Power PC based SOC which has 4 channel PCIe interface, 2 channel SAS interface, 2 channel FC interface, 16 channel Flash Controller Interface and DDR3. My role is to verify SAS to DDR3 and SAS to FCI data path along with Top level DV environment development.

***Digital Block design and DFT Scan Design for RF, PMIC Chipsets:*** RXPLL digital interface block, TX top level block and RX top level block design and RTL coding in Verilog, DFT scan insertion, Synthesis using DC, FV using Verplex and verify the DFT scan using Tetramax. Verify the RX PLL digital block using AMS simulations. Secure RTC block micro architecture, design and RTL coding using Verilog. Bug fixes for the existing designs Temperature Alarm, XOADC

***Secure RTC and Temperature Alarm design for PMIC Chipsets:*** Micro architecture, design and Verilog RTL coding for Secure RTC and Temperature alarm blocks.

***Verification of Secure RTC, Temp Alarm, XOADC sinc2 Filter, Digital Keypad, TS/HKADC, Interrupt Controller, I2CSSBI and SSBI blocks:*** DV environment creation, test plan creation, executing the test plan for all the blocks.

***Verification of 6 Sub Systems using System Verilog:*** Lead a team of 2 to 3 engineers. Designed and implemented coverage based verification environment to verify highly configurable Sub Systems. Assertion based verification for configurable sub blocks using PSL assertions.

***Dorothy Print FPGA:*** Modified the existing ASIC RTL to support FPGA. Designed VBUSP2AHB an AHB2USB bridges for using ARM Board. FPGA synthesis using SynplifyPro. Equivalency check between RTL and FPGA net list using LEC. Board level validation done at customer’s site in USA.

***PCI Express Bridge Verification:*** Development of chip level Verification, Random testing setup, Data checker and Rule/Ordering checker. Also managed the whole team including design team.

***PCI Express Core Design and Verification using Verilog and C:*** Full chip micro architecture, Verification environment setup, and Verilog based test bench and test matrix creation. Managing team of 12 engineers.

***USB2.0 OTG Core Verification using Verilog*:** Development of Verification environment which consists of test bench, test matrix along with chip level validation test vectors. Lead the Verification team.

***8032 Microcontroller based Ethernet to 4 Serial and 1 Parallel port SOC ASIC using Verilog:*** Designed and developed Verilog based Verification environment. Also generated Production test vectors for the ASIC.

***USB2USB Link, USB2Ethernet Link, USB2Serial/Parallel Ports, PCI2Serial/Parallel Ports verification Using Verilog:*** Development of PCI Target, PCI Initiator, PCI Protocol Checker, Arbiter, USB, Ethernet, UART and Parallel port BFMs, Test bench, Test matrix Creation. Also Production Test vector generation for ASICs. All these projects executed simultaneously, managed complete verification activities including Gate level simulations of all projects. Also Validation of ASICs.

***Design and Verification of PCI-X Rev1.0b using Verilog:*** Micro Architecture, Design and Verification of PCI-X reg1.00b IP Core. Also verified this core on FPGA. Lead the team of 4 Engineers. ASIC synthesis and STA was also done.

***DFT Verification for iCL, iATOM, CAM and DRAM using Specman:*** Complete RTL DFT verification using Specman was done on iCL, iATOM, CAM and DRAM chipsets. DFT verification includes Memory BIST, ATPG, SCAN, JTAG boundary Scan, Nand tree test, PLL testing along with CAM and DRAM testing. This

***Bluetooth Baseband Core Design with PCI and AMBA ASB interface:*** Micro Architecture and Design of the Bluetooth Baseband core. Developed the core in Verilog RTL. Verified this RTL on FPGA using both PCI Rev2.2 based FPGA and AMBA ASB based FPGA. Integrated with trimedia chipset. ASIC Synthesis and STA was done for the trimedia chipset. Lead the design team of 2 engineers.

***Synthesizable PCI Random transaction generator Design:*** Design and Verification of PCI random transaction generator. RTL validation was done on FPGA.

***DVP to PI Bridge RTL development, Full chip verification and Synthesis:*** Designed and developed in Verilog RTL DVP to PI bus bridge for 2nd generation Trimedia VLIW processor based set top box chip set. Full chip level verification and ASIC synthesis was done.

***1394a Core RTL development:*** Designed and developed Verilog RTL code for 1394a Transmitter block. Block level verification was done.

# **EDUCATION**

BE-Electronics and Communications Engineering: Kuvempu University, Karnataka, India, April 1998